Payload Interface Electronics (PIE) – Modularity at the Payload Level (SSC14-P4-6)

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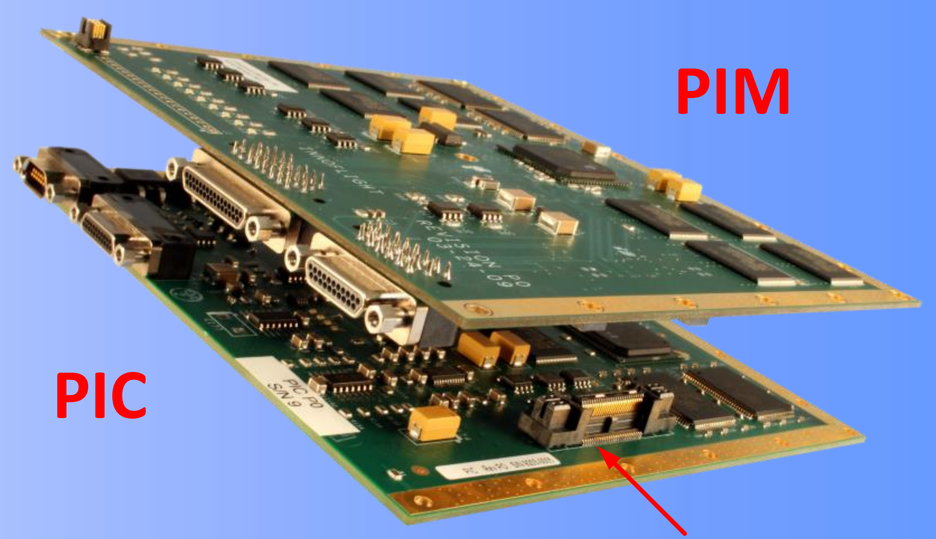
A PIE slice is a standard payload processing element designed to support an experiment to a simplified bus interface

- Payload Interface Controller (PIC): Standard full-featured processing board dedicated to payload application
- Payload Interface Mezzanine (PIM): Unique interface board for specific I/O or other payload support requirements
- The PIM stacks on top of the PIC, and both are installed into a single enclosure called a "Slice"
- Several slices constitute a "PIE stack"
- Slices are designed to stack onto each ether to create a single unit with multiple slices
- Every PIE slice provides the payload with a complete support platform including: high performance processing, complete with a BSP (Board Support Package), auto-coding support for Matlab and National Instruments high level design software, power control, power monitoring, fault detection & mitigation, telemetry, on-board data storage, high speed serial and Ethernet interfaces, support for direct downlink modulation, data encryption, and user designed hardware interfaces.



PIE Slice

Flight Proven = TRL-9

PIE Stack

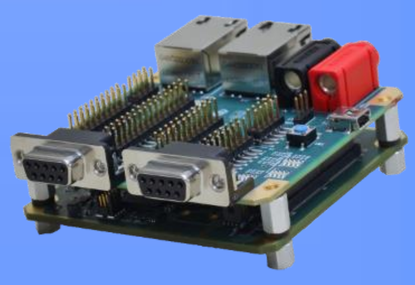
Benefits of the PIE Approach

- Isolate the bus from low level payload management; reduce payload burden on the bus
- Simplify bus to payload interfaces; avoid the rats-nest of adapter to adapter boxes
- Simplify bus C&DH software; no need for C&DH to perform low level payload operations
- Distributed processing approach -> higher quality, higher reliability software
- Ideal for missions with multiple, disparate payloads/experiments
- Streamlined mission development; less inter dependency between software development
- Significant reduction of payload to spacecraft integration timeline
- Recurring engineering cost (hardware and labor) limited to PIM and payload concept of operations (CONOPS)

PIE philosophy facilitates independent evolution of PIC and PIM designs to address technology advancements in electronics, software, spacecraft and payload design

- Initial SmallSat flight unit (multiple slices inc. SSDR) successfully on-orbit and functioning for over three years
- Latest engineering units include high-performance multi-core processors, Linux BSP, SpaceWire, SGMII Gigabit Ethernet and CAN. Ideal for hosted payloads
- Next generation technology introduces advanced capabilities including secure boot, encryption, on-orbit reconfiguration, software and hardware processing accelerators
- CubeSat-variant with lower SWaP supports multi-mission busses and CubeSats supporting multiple payloads

Next Generation PIE Engineering Unit



PIE Capability in CubeSat Form Factor

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